PATENT #7
LW

IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

APPLICANTS:	Nalini Ranjan and Xiaoyi Guo
PATENT NO.:	6,005,412
ISSUE DATE:	December 21, 1999
SERIAL NO.:	09/057,047
FILING DATE:	April 8, 1998
TITLE:	AGP/DDR INTERFACES FOR FULL SWING AND REDUCED SWING (SSTL) SIGNALS ON AN INTEGRATED CIRCUIT CHIP
ATTY. DKT. NO.:	3156

APPROVED
NOV 29 2001
FOR THE DIRECTOR OF USPTO
Marietta Joyce

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, DC. 20231, on the date shown below:

Dated: 4 Feb. 2000 By: _____
Greg T. Sueoka, Reg. No.: 33,800

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC. 20231

ATTENTION: DECISION AND CERTIFICATE OF CORRECTION
BRANCH OF THE PATENT ISSUE DIVISION

REQUEST FOR CERTIFICATE OF CORRECTION

SIR:

The following error, as more fully described below, appears in this patent.

☐ The Applicant submits that no fee is due for correction of the errors made by the Patent and Trademark Office; OR,

☒ The error occurred in good faith. Correction thereof does not involve such change in the patent as would constitute new matter or would require re-examination. A

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Certificate of Correction is requested. Enclosed herewith is payment in the amount of $100.00 to cover the fee for this Certificate of Correction.

Attached hereto are duplicate Forms PTO-1050, with at least one copy that is suitable for printing.

Applicant kindly requests the following change:

Figure 2A. The line labeled "234" should couple the line 210 to the clock input of flip-flop 212-3.

Please send the Certificate to:

GREG T. SUEOKA
Fenwick & West LLP
Two Palo Alto Square
Palo Alto, CA 94306

Respectfully submitted,
Nalini Ranjan and Xiaoyi Guo

Dated: 4 Feb 2000

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US006005412A

United States Patent [19]

Ranjan et al.

[11] Patent Number: 6,005,412

[45] Date of Patent: Dec. 21, 1999

[54] **AGP/DDR INTERFACES FOR FULL SWING AND REDUCED SWING (SSTL) SIGNALS ON AN INTEGRATED CIRCUIT CHIP**

[75] Inventors: **Nalini Ranjan**, Sunnyvale; **Xiaoyi Guo**, Santa Clara, both of Calif.

[73] Assignee: **S3 Incorporated**, Santa Clara, Calif.

[21] Appl. No.: **09/057,047**

[22] Filed: **Apr. 8, 1998**

[51] **Int. Cl.**[6] **H03K 19/0175**

[52] **U.S. Cl.** **326/63**; 326/38; 326/96; 326/86

[58] **Field of Search** 326/37, 38, 82, 326/83, 86, 90, 93, 95, 96, 98

[56] **References Cited**

U.S. PATENT DOCUMENTS

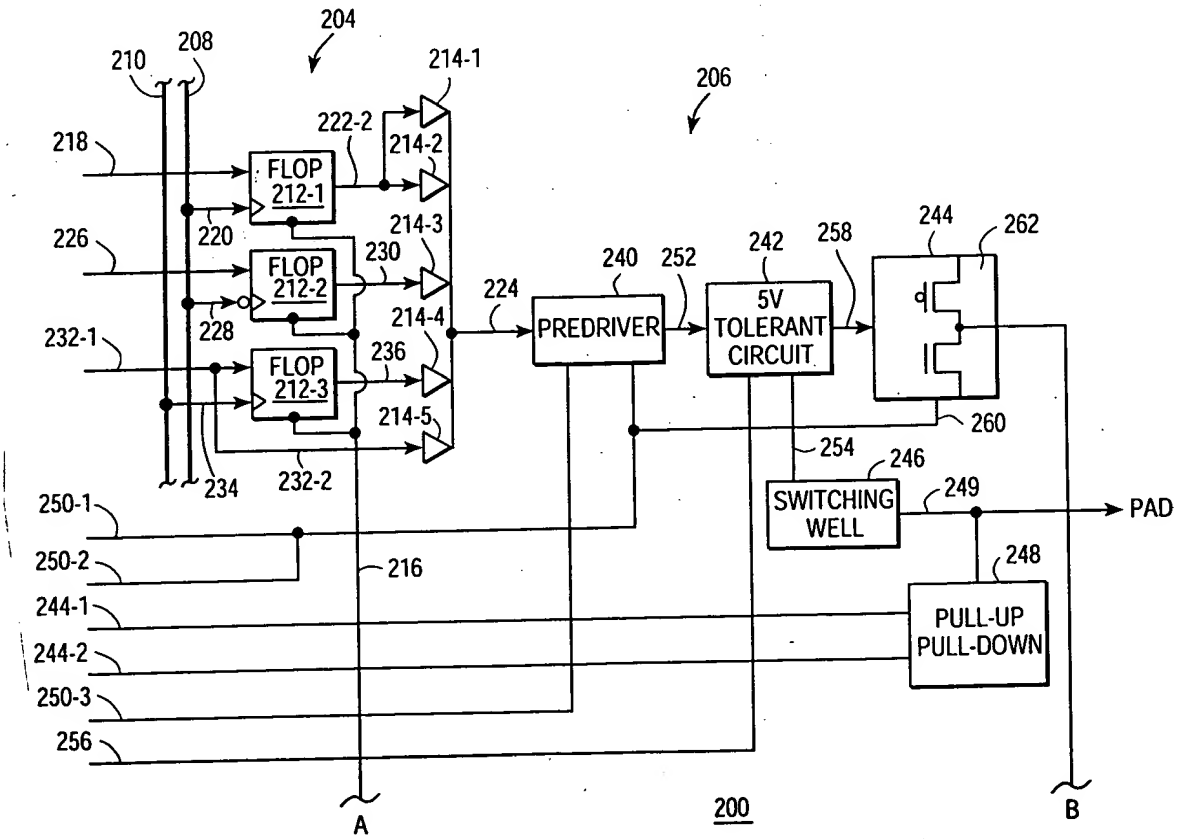
5,017,813	5/1991	Galbraith et al.	326/38
5,530,379	6/1996	Konishi et al.	326/68
5,646,553	7/1997	Mitchell et al.	326/37
5,736,867	4/1998	Keiser et al.	326/38
5,804,987	9/1998	Ogawa et al.	326/37

Primary Examiner—Michael Tokar
Assistant Examiner—Don Phu Le
Attorney, Agent, or Firm—Fenwick & West LLP

[57] **ABSTRACT**

An I/O interface includes latches, clocks, and conditioning circuits implemented in a custom physical layout to produce a reliable and flexible interface to high frequency busses running a plurality of protocols and signal specifications. Three clock trees are used to synchronize the buffering and conditioning of input/output signals before sending such signals to a pad or core. The clock trees are implemented via custom layouts to allow tight control of clock/strobe parameters (e.g., skew, duty cycle, rise/fall times). Two of the clock trees are local to the I/O interface and trigger a plurality of output latches configured on-the-fly to buffer output data signals from the core in asynchronous or synchronous mode. In the synchronous mode, a clock/strobe could be either edge-centered or window-strobe with respect to the data. The third clock tree distributes clock/strobes from an external source and is used to trigger a plurality of input latches configured on-the-fly to buffer input data from the pad in either a window-strobe mode or an edge-centered mode. The I/O interface also includes conditioning circuits that condition the I/O signals to be compliant with AGP/DDR protocols, as well as, full swing, reduced swing (SSTL), and TTL signal specifications.

15 Claims, 13 Drawing Sheets



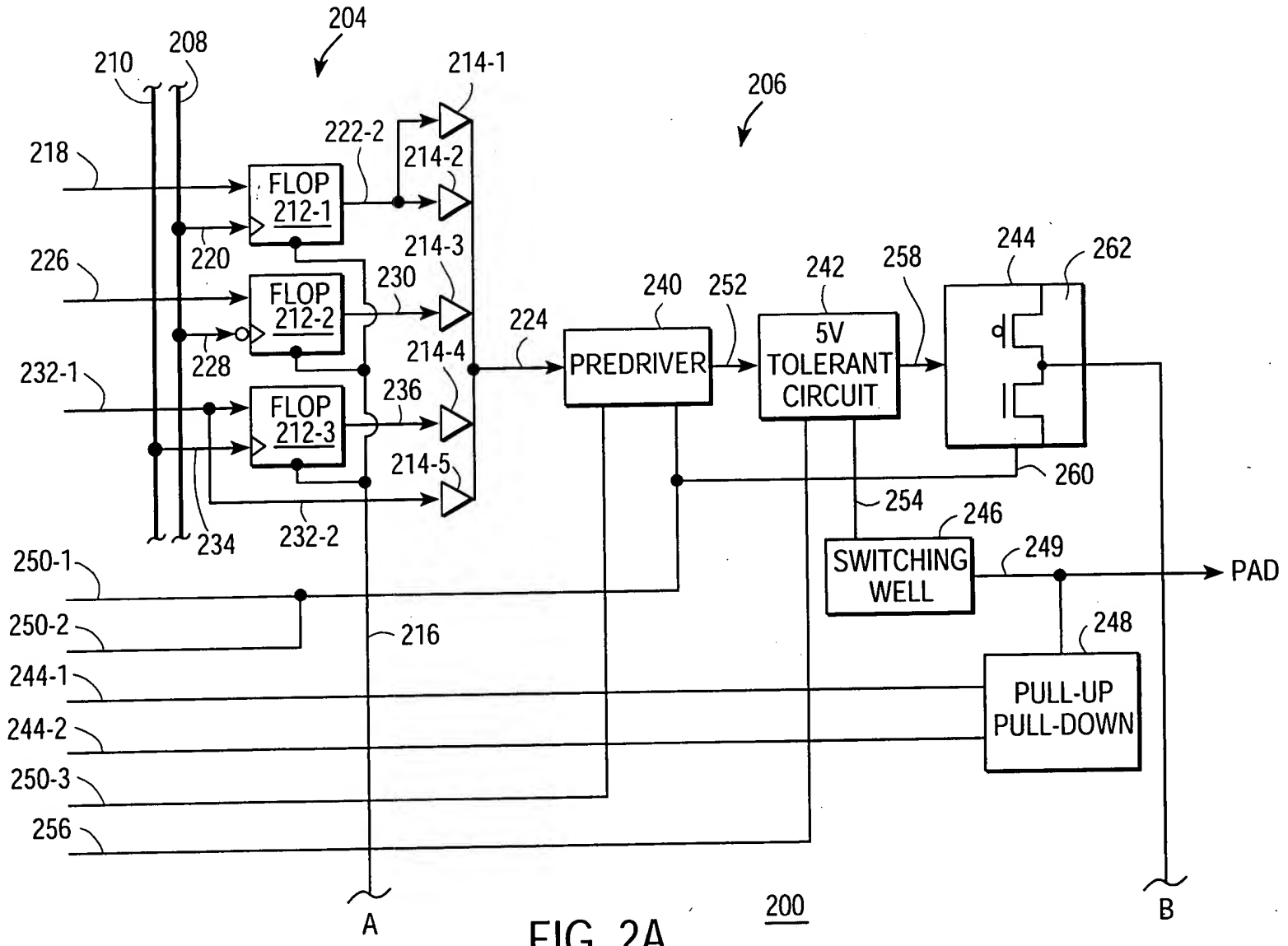

204
206
210
208
214-1
222-2
214-2
218
FLOP
212-1
220
214-3
226
230
FLOP
212-2
228
214-4
232-1
236
FLOP
212-3
214-5
234
232-2
224
PREDRIVER
240
252
5V
TOLERANT
CIRCUIT
242
258
244
262
260
254
246
SWITCHING
WELL
249
PAD
248
PULL-UP
PULL-DOWN
250-1
250-2
216
244-1
244-2
250-3
256
A
B
200

FIG. 2A

United States Patent [19]

Ranjan et al.

[11] **Patent Number: 6,005,412**

[45] **Date of Patent: Dec. 21, 1999**

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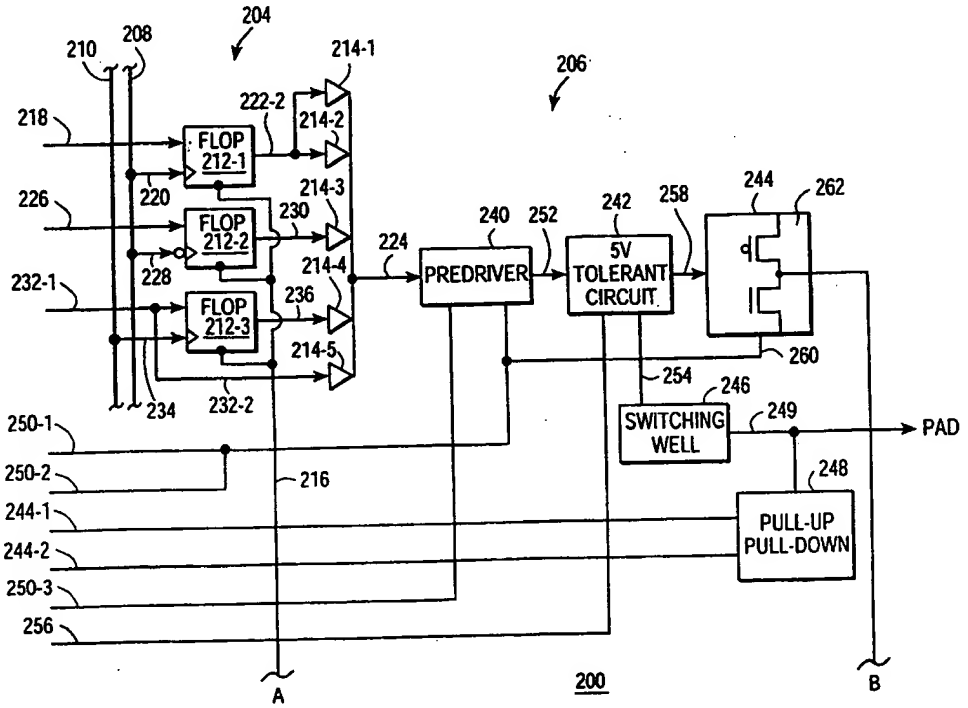

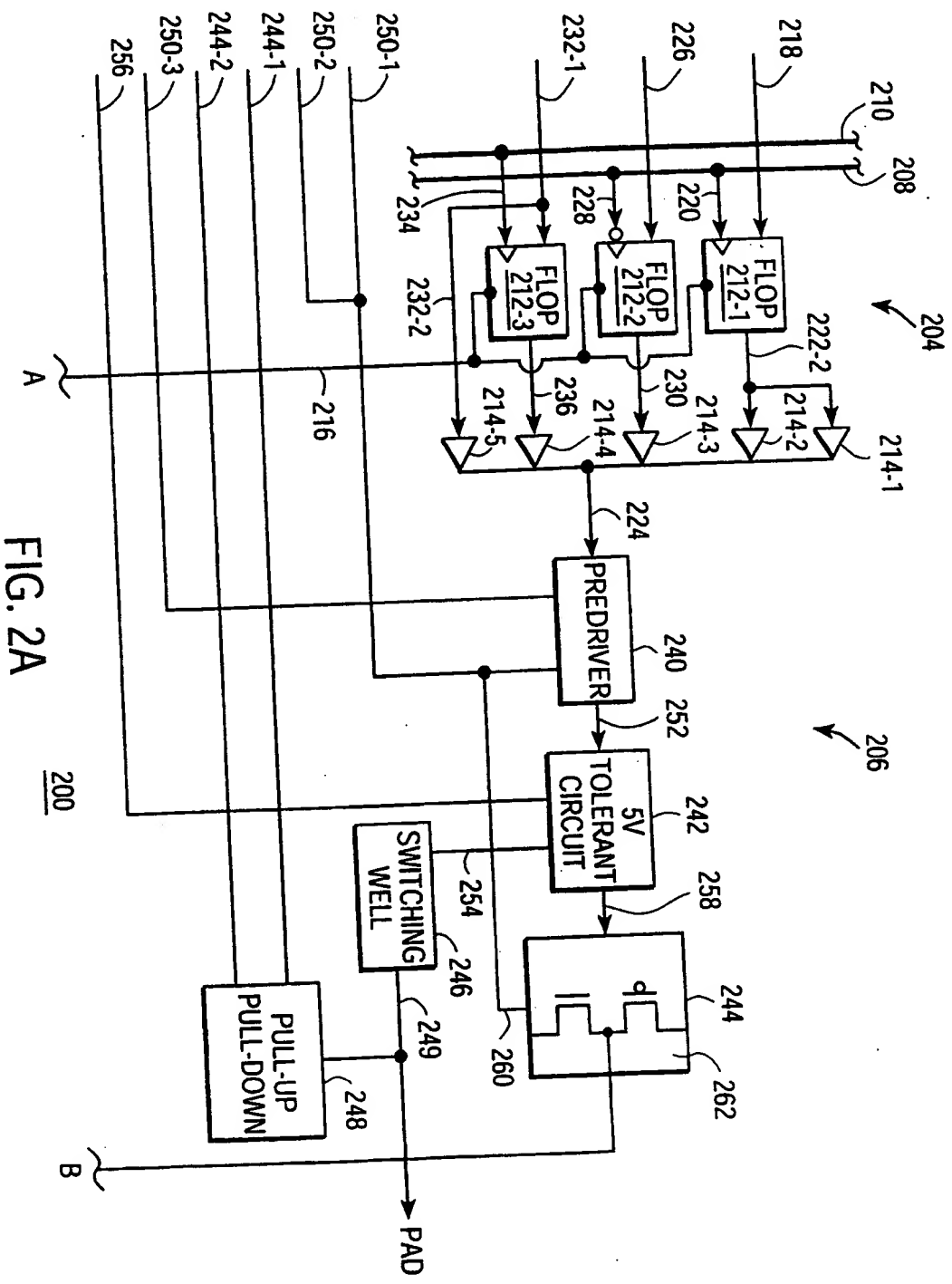
FLOP 212-1
FLOP 212-2
FLOP 212-3
PREDRIVER
5V TOLERANT CIRCUIT
SWITCHING WELL
PULL-UP PULL-DOWN
PAD
A
B
200
204
206
208
210
214-1
214-2
214-3
214-4
214-5
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222-2
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250-1
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250-3
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260
262

FIG. 2A

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

Page 1 of 3

PATENT NO. : 6,005,412

DATED : December 21, 1999

INVENTOR(S) : Nalini Ranjan and Xiaoyi Guo

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Figure 2A. The line labeled "234" should couple the line 210 to the clock input of flip-flop 212-3.

Atty

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PATENT NO. 6,005,412

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,005,412
DATE : Dec. 21, 1999
Inventor : Ranjan et al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing an illustrative figure, should be deleted and substitute therefore the attached title page.

Delete Figure 2A and substitute therefore the Figure 2A as shown on the attached page.

UNITED STATES PATENT AND TRADEMARK OFFICE

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PATENT NO : 6,005,412
DATE : Dec. 21, 1999
Inventor : Ranjan et al

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The title page showing an illustrative figure, should be deleted and substitute therefore the attached title page.

Delete Figure 2A and substitute therefore the Figure 2A as shown on the attached page.